What is claimed is:

1. A method for simulating hardware circuits during which voltages are calculated at a plurality of circuit nodes, comprising the steps of:
   (a) carrying out a first DC-simulation run at the begin of a functional cycle,
   (b) carrying out a second DC-simulation run at the end of said cycle,
   (c) comparing simulated values from both runs at respective circuit nodes, and
   (d) storing mismatch information about static error afflicted nodes at which the calculated values differ by more than a predetermined first threshold value.

2. The method according to claim 1 further comprising the steps of:
   (e) putting out said mismatch information for a manual correction,
   (f) carrying out a transient analysis covering the same functional cycle after correction,
   (g) comparing calculated values from said analysis with calculated values from said first or second DC simulation run at respective circuit nodes, and
   (h) storing mismatch information about dynamic error afflicted nodes at which the calculated values differ by more than a predetermined second threshold value.

3. The method according to claim 2 further comprising the step of automatically correcting dynamic errors in a simulation input file.

4. The method according to 3 claim further comprising the step of performing an iterative hardware simulation with the corrected simulation input file.

5. The method according to claim 1 comprising the step of setting the START TIME prior to the begin of a functional cycle.

6. The method according to claim 1 in which the hardware is built according to silicon-on insulator (SOI) technology.

7. A computer system having installed program means comprising program code portions for performing the steps:

(a) carrying out a first DC-simulation run at the begin of a functional cycle,

(b) carrying out a second DC-simulation run at the end of said cycle,

(c) comparing simulated values from both runs at respective circuit nodes, and

(d) storing mismatch information about static error afflicted nodes at which the calculated values differ by more than a predetermined first threshold value.

8. The computer system according to claim 7 further comprising program code portions for performing the steps:

(e) putting out said mismatch information for a manual correction,

(f) carrying out a transient analysis covering the same functional cycle after correction,

(g) comparing calculated values from said analysis with calculated values from said first or second DC simulation run at respective circuit nodes, and

(h) storing mismatch information about dynamic error afflicted nodes at which the calculated values differ by more than a predetermined second threshold value.

9. A hardware testing computer system having installed program means comprising program code portions for performing the steps:

(a) carrying out a first DC-simulation run at the begin of a functional cycle,

(b) carrying out a second DC-simulation run at the end of said cycle,

(c) comparing simulated values from both runs at respective circuit nodes, and

(d) storing mismatch information about static error afflicted nodes at which the calculated values differ by more than a predetermined first threshold value.

10. The computer system according to claim 9 further comprising program code portions for performing the steps:

(e) putting out said mismatch information for a manual correction,

(f) carrying out a transient analysis covering the same functional cycle after correction,

(g) comparing calculated values from said analysis with calculated values from said first or second DC simulation run at respective circuit nodes, and

(h) storing mismatch information about dynamic error afflicted nodes at which the calculated values differ by more than a predetermined second threshold value.

11. Computer program comprising code portions adapted for performing the steps below when said program is loaded into a computer system:

(a) carrying out a first DC-simulation run at the begin of a functional cycle,

(b) carrying out a second DC-simulation run at the end of said cycle,

(c) comparing simulated values from both runs at respective circuit nodes, and

(d) storing mismatch information about static error afflicted nodes at which the calculated values differ by more than a predetermined first threshold value.

12. The computer program according to claim 11 further comprising program code portions for performing the steps:

(e) putting out said mismatch information for a manual correction,

(f) carrying out a transient analysis covering the same functional cycle after correction,

(g) comparing calculated values from said analysis with calculated values from said first or second DC simulation run at respective circuit nodes, and

(h) storing mismatch information about dynamic error afflicted nodes at which the calculated values differ by more than a predetermined second threshold value.

13. Computer program product stored on a computer usable medium comprising computer readable program for causing a computer to perform the method comprising:

(a) carrying out a first DC-simulation run at the begin of a functional cycle,

(b) carrying out a second DC-simulation run at the end of said cycle,

(c) comparing simulated values from both runs at respective circuit nodes, and

(d) storing mismatch information about static error afflicted nodes at which the calculated values differ by more than a predetermined first threshold value.

14. The computer program product according to claim 13 wherein said method further comprises performing the steps:

(e) putting out said mismatch information for a manual correction,

(f) carrying out a transient analysis covering the same functional cycle after correction,

(g) comparing calculated values from said analysis with calculated values from said first or second DC simulation run at respective circuit nodes, and

(h) storing mismatch information about dynamic error afflicted nodes at which the calculated values differ by more than a predetermined second threshold value.